

WorkRequests by Request Number

<i>Requisition</i>	<i>Requester</i>	<i>Requested</i>	<i>Required</i>	<i>WBS</i>	<i>Request</i>	<i>Assigned1</i>	<i>Completed</i>
EED-00052	Bob DeMaat	2/12/2002	2/22/2002	CBX	<p>Under the direction of Claudio Rivetta, assemble 8 boxes that will have 4 transistors each. These will be used to conduct test of the radiation tolerance of the transistors.</p> <p>The boxes will have connectors for power and signals.</p>	Wayne Johnson	7/1/2002
EED-00053	J. Conrad	4/24/2001	6/1/2001		<p>Would like analog engineer familiar with PMT bases to try to help understand failures in MiniBoone PMT's. This is a bit of a crisis. Contact persons are:</p> <p>Prof. Janet Conrad/Bonnie Fleming/</p> <p>Work may be at New Muon Lab of Lab 3/S. Pordes.</p> <p>Date required is ASAP</p>	Claudio Rivetta	5/23/2001
EED-00054	Hugh Montgomery	8/22/2001		DIO	<p>Redesign MFC module.</p> <p>Boris Baldine</p> <p>To confirm previous e-mail request.</p> <p>Note from Ray Yarema: Had many problems; there may still be unfound problems.</p>	Boris Baldine	7/25/2002
EED-00055	Bob DeMaat	2/12/2002	2/18/2002	CBX	<p>Under the direction of Stan Orr, a technician is needed to evaluate 12 power supplies that are suspected to be bad. Ones that test good can be returned to service. Ones that test bad may have an attempt made to repair them or they can be sent to the manufacturer for repair.</p> <p>These are 1 kilowatt, 400 Hz linear supplies manufactured b PEI. This will require about one week of technician labor. See attached procedure. (in manual)</p>	Steve Morrison	7/24/2002
EED-00056	Bob Tschirhart	3/15/2002	12/2/2002	PAL	<p>Design Qie based readout test board for CKM to test ping pong of 2 Qie's.</p>	Charlie Nelson	10/31/2002
EED-00057	Bob Tschirhart	3/15/2002	8/2/2002	PAL	<p>Design VVS prototype PMT Base for CKM.</p> <p>Need 8 channels working for test beam by end of summer 2002.</p>	Sten Hansen	8/30/2002
EED-00058	Bob Tschirhart	3/15/2002	8/2/2002	PAL	<p>Design of 8 channels of phototube readout with qie.</p>	Kwame Bowie	1/30/2003
EED-00059	Paul Mantsch	6/11/2002	11/1/2002	TFM	<p>About seven or eight years ago Merle Watson and Tom Droege built a demonstration Geiger counter unit for the Auger project. It had two counters, each gibinv a different tone a fifth apart. This thing has been an enormous success.</p> <p>It has been used in uncounted Auger talks and even went up in a hot air balloon in Aspen. We would like to build two more of these for use at the Auger Observatory visitors center and for presentations.</p> <p>The first unit was hand wired . It would probably be best to layout a PC board as we may want more in the future. We can start by making anew schematc, bill of material and layout.</p> <p>Note that this is low priority compaterd to other Auger work already underway in the EED.</p> <p>We have ther original schematics and the existing unit that can be used to start this work.</p>	Xinyi Chen	12/30/2003

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EED-00060	Jim Steimel	6/14/2002	12/12/2002		<p>Perform a design study on a digital, direct RF feedback system for the main injector RF cavities. The systems input will be from the cavity gap monitor. The signal will be filtered and then drive the RF power amplifier. This signal will be optimally filtered to provide the best possible beam induced voltage suppression and remain stable. The minimum amount of suppression should be 40dB at the first harmonic of the beam's rotation frequency off the fundamental.</p> <p>At the conclusion of the design study (assuming it is positive), a prototype design should exist. The design would include simulations of the global process to verify its effectiveness. It would also include simulations of key, complicated subprocesses. A detailed schematic of the system should be completed, and all software necessary to operate the prototype should be tested. Also, a cost estimate of parts, time and labor to construct and commission the system should be created.</p>	Claudio Rivetta	
EED-00061	Bob Webber	6/14/2002	8/1/2002		<p>Develop coherent and soundly engineered Booster Fast Beam Loss Monitor System. Existing Fast BLMs are a hodgepodge of scintillator /pmt devices with random cabling and no coherent signal handling system.</p> <p>Phase I is to help develop defined requirements and specs. By 8/1/02 and to be reviewed at end of phase I.</p> <p>Phase II is to engineer ad solution</p> <p>Phase III is to install and commission that solution</p> <p>Work will be done with guidance and inputs from Bob Webber, Jim Lackey, and Ray Tomlin of the Booster Group</p>	Marcus Larwill	
EED-00062	S. Pordes	6/17/2002	10/17/2002		<p>Analyze Ionization Profile Monitor physics and performance. Issues include: stability, accuracy, longevity, dynamic range; Variables include: beam current, beam density, residual vacuum; Parameters include: gain of MPC, collection of ions or electrons, E & B fields applied.</p> <p>Investigate available MCP's (Multi-channel plates)</p> <p>Look at feasibility of application to Tevatron. Work closely with J. Zagel who has built and is developing these systems.</p> <p>Note from Ray Yarema - Charlie has other commitments. He can work on IPM's 25% from now until 10/1, then 50% until 12/31. First work shall define scope and magnitude of the project. Come up with project plan.</p>	Charlie Nelson	11/8/2002
EED-00063	J. Zagel	6/17/2002	9/17/2002		<p>1) Devise upgrade path for control system of pbar flying-wires. Controls include motor-control, data acquisition and control. Upgrade path must be consistent with and applicable to Main Injector and Tevatron flying-wire systems.</p> <p>2) A request for implementation will follow.</p> <p>Note:</p> <p>a. Work requires close interfacing with existing experts</p> <p>b. Part of (1) will involve familiarizing with present pbar system.</p>	Craig Drennan	

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EED-00064	Jon Kotcher	7/12/2002	8/7/2002		<p>In one of the critical D0 systems for Run 2b -- the calorimeter/track match hardware level trigger system -- we have a problem related to latency that needs to be seriously investigated prior to the Run 2b review cycle that begins August 12. One way to address the problem is to increase the depth of the muon pipeline. We've had preliminary discussions with Boris about it, and it appears that there are some promising ideas here, but a relatively minor amount of engineering is required to study them.</p> <p>Boris feels that, with the help of Tom Fitzpatrick and Sten Hansen -- and all at a reasonably low duty cycle -- the three of them could solve this in 4-6 weeks time. He has offered to help us with this -- Tom and Sten are apparently on board as well, as I understand it. Naturally, we need to have an answer in hand prior to the review, so time is somewhat pressing for this.</p> <p>Can we arrange for the necessary fraction of their time to accomplish this?</p>	Boris Baldine	9/1/2002
EED-00065	Paul Mantsch	5/30/2002	10/1/2002	TFM	<p>Complete design, fabrication, and testing of 150 Micro-TPCB boards and enclosures. The specification for the Micro-TPCB is attached. The Micro-TPCB has been redefined from the TPCB originally produced for the Engineering Array by EED in order to improve Integration with the Unified Board that is being produced by College de France.</p> <p>PPD EED shall consult with Pierre Auger Argentine Collaborations to ensure that the design is suitable for production in Argentina. The 1500 Micro-TPCB units required to complete the array will be produced in Argentina, and all units will be maintained by staff at the Pierre Auger Southern Site in Malargue, Argentina.</p>	Kwame Bowie	1/3/2003
EED-00066	G. Tassotto	6/16/2002			<p>1.) MiniBooNE Instrumentation: 2 Techs 50% from 6/10 to 6/21/02</p> <p>2.) Sy-120 Instrumentation : 2 techs 50% from 6/24 to 7/5/02</p> <p>3.) Assembly of detectors and electronics: 2 techs 30% from 7/8 to 7/26/02</p>	Wayne Johnson	12/30/2003
EED-00067	Ken Nelson	6/20/2002	10/1/2002	PAL	<p>Engineer and technical support are needed to work on the R&D of a commercial component based charge measurement circuit. The specific works include evaluating a commercial ADC chip AD6644/AD6645 or similar component, designing laying out and fabricating a printed circuit board with integrator circuit developed by the University of Virginia group plus the ADC chip and an FPGA chip. The ADC data will be stored in the memory inside FPGA and should be able to be read out to a computer. The ADC data output should be compatible with the PCI card being developed by Bill Haynes for readout of the QIE during the CKM fall '02 beam test at TJNAL.</p>	Jin-Yuan Wu	2/17/2003
EED-00068	Rick Coleman	9/5/2002			<p>SWIC Scanners - old style scanners in Meson need to be replaced by SWIC scanners currently installed in the proton, neutrino (muon) switchyard lines. This applies to F2, F3, M01, M-Test and M-Center. Remove, Test, Install, (Controls Department - Al Franck) (Terry Kiper knows where the old ones are - copy Tassotto's list).</p> <p>Rick Coleman, Gianni Tassotto and Al Franck will agree (tomorrow) on the exact list of scanners to be moved.</p>	Wayne Johnson	11/30/2003

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EED-00069	Hogan Nguyen	9/17/2002	2/1/2003		Design of a 16-channel amplifier/discriminator board, which would be tested first in one of our 20-channel prototypes. Below are some considerations: (1) Electronics gain of 20 mV/uA. Our straws are at ground. The wires will be about - 1900 volts, so blocking caps will be needed. (2) An adjustable electronics threshold of 25-50 mV (3) Output pulsewidth of 30 nsec. and insensitive to multiple-pulsing within a straw. (4) Output pulse rise time of 4-5 nsec. (5) 16-channel board with edge-card connector (6) The LV, and the HV power distribution to be routed on buses built into the chamber. (7) Discriminator Output logic--should be LVDS or ECL. Will test the prototype board with the LRS3377, which accepts ECL. It should also be compatible with the CKM TDC. (8) Packaging--We are somewhat biaded against ASICS. Considering putting TDC directly on their front end.	Mark Kozlovsky	
EED-00070	Craig McClure	9/13/2002	12/1/2002		Assemble and test quantity 10 Switchyard 120 BPM sample and hold modules. Job includes assembly and test of circuit board, install circuit board into 19" rack mountable chassis, install and wire power supply into chassis. Inventory and purchase components as necessary.	Wayne Johnson	2/1/2003
EED-00071	Peter Prieto	8/21/2002	8/30/2002	FNO	Analyze failure mode of minicircuits switch attached. These are used for Recycler BPM test inputs. Failed parts provided (more on request) - radiation could be cause. Circuit diagram also provided - circuit on request. (Call S. Pordes if needed x3603, 722-2167)	Marcus Larwill	2/1/2003
EED-00072	Eugene Lorman	9/26/2002	11/28/2002	FNO	See attached. RF clock to TTL clock Converter	Tom Fitzpatrick	1/1/2003
EED-00073	Yuriy Pischalnikov	10/4/2002	12/20/2002	FNO	Design and production of 25 bases for R5380 PMT'S for Beam Lost Monitor as a part of upgrading Flying Wires Beam Profile Monitor for RUNII, See attached for more information.	Terry Kiper	11/30/2003
EED-00074	Linda Bagby	10/29/2002			This task is for John Foglesong, supported by Linda Bagby. A Low Voltage Power Supply system is to be designed for the RunIIb Silicon Detector Upgrade Interface Board crates. John will be responsible for the design, documentation, procurement of parts, installation, and testing of the systems. Eight systems will be procured and installed in the experiment. A failure mode analysis and safety review will be performed on the system to obtain design approval for production. The upgrade design will include the moving of the supplies from the Cathedral area to a more accessible location and minimization of the number of fuses required for the system. Two spare systems will be constructed in addition to the eight required systems. The spares will be installed in test stands prior to the release of the production order. A refurbished RunIIa power supply test stand will be used to test the production units. System specifications and project schedule are attached. (see binder)	John Foglesong	

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EED-00075	Linda Bagby	10/30/2002			<p>This task is for John Foglesong, supported by Linda Bagby. A Power Supply system is to be designed for the RunIIb Silicon Detector Upgrade Adapter cards. John will be responsible for the design, documentation, procurement of parts, installation, and testing of the systems. Eight systems will be procured, tested and installed in the experiment.</p> <p>Supply accessibility will be a key design feature. Two spare systems will be installed in test stands prior to the release of the production order. A failure mode analysis and safety review will be performed on the systems to obtain design approval for production. A refurbished RunIIa power supply test stand will be used to test the production units.</p> <p>System specifications and project schedule are attached. (see binder)</p>	John Foglesong	
EED-00076	Linda Bagby	11/20/2002			<p>This task is for John Foglesong, supported by Linda Bagby. The adapter card ring (horseshoe) is a circular structure that is used to mount the Adapter cards, Radiation monitoring junction cards, and temperature monitoring junction cards. The assignment is to design, document, procure, test and install the structure.</p> <p>The design must:</p> <ol style="list-style-type: none"> 1. Minimize the disturbance of the existing cable plant. 2. Address Adapter card cooling issues. 3. Minimize noise coupling. <p>A prototype structure will be constructed to verify design parameters.</p> <p>See previous drawings for structure specifications at \\D0server4\users\fogie.900811-16.ps</p> <p>The project schedule is attached (see original). See WBS 1.1.2.21.1.8 and 1.1.2.21.2.5 for design work. See WBS 1.5.1.8.1 for installation work.</p>	John Foglesong	
EED-00077	Marvin Johnson	11/26/2002	5/1/2003		<p>Design and develop an 'LVDS Pickoff Board' for use with the Level 1 Trigger system at D0. This board need interpose itself between 50 twisted pair cables (40 data, 10 clock) and the input connector of DFE boards without interfering with the transmission or timing of the data into the DFE at the full aggregate bandwidth of 15 Gb/sec. The board shall provide a multiplexing capability to allow connection of at least 64 channels of logic analyzer to selectable subsets of the 280 data bits carried over the twisted pairs. Upon completion of design manufacture six for use at D0.</p> <p>Project requirements reviewed and some features removed Feb. 2003. Original board count of 10 reduced to six at this time. Revised specification document due 3/15/2003, finish date moved to 5/1/2003 based upon schedule and requirements changes. See notes below.</p>	John Anderson	
EED-00078	S. Pordes	12/5/2002	3/31/2003		<p>Modify programs for 080 and 8004 cards used in MultiBus systems. New program will drop support for 2 BLM systems in one crate while maintaining 1BPM & 1BLM and 1BLM in one crate capability.</p> <p>(Objective is to allow space for improvements in turn-by-turn BPM readout.)</p> <p>Support tests and installation of new code.</p>	Alan Baumbaugh	

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EED-00078	S. Pordes	12/5/2002	3/31/2003		<p>Modify programs for 080 and 8004 cards used in MultiBus systems. New program will drop support for 2 BLM systems in one crate while maintaining 1 BPM & 1 BLM and 1BLM in one crate capability.</p> <p>(Objective is to allow space for improvements in turn-by-turn BPM readout)</p> <p>Support tests and installation of new code.</p>	Alan Baumbaugh	
EED-00079	Peter Prieto	12/5/2002			<p>Provide manpower and organization to remove 440 store (if needed), deliver to Prep, reinstall (200) and assist with in-place testing: ~440 BPM preamplifier modules from the Recycler Ring. The work is to be done in the shutdown starting Januar 13. Mods done by computing.</p>	Wayne Johnson	
EED-00079	Peter Prieto	12/5/2002			<p>Provide manpower and organization to remove (440) store (if needed), deliver to Prep, reinstall (200) and assist with in-place testing:</p> <p>~440 PBM preamplifier modules from the Recycler Ring.</p> <p>The work is to be done in the shutdown starting Jan. 13.</p> <p>Mods done by Computing.</p>	Wayne Johnson	1/24/2003
EED-00080	S. Pordes	2/20/2003	3/13/2003		<p>See if it is possible to modify the PMT base designed by S. Hansen for Y. Pischalnikov and used in the Beams Flying wire systems such that one can gate on and off the voltage between the photocathode and the first dynode stage. The off state is the default; the on state would last for 3 microsecond periods every 7 or 21 microseconds as feasible for a total time of 500 microseconds - this would be exercised every few minutes at most. The 'on' voltage between the photocathode and the first dynode need not be greater than 200 volts. The switching time (off-on and on-off) should not be more than 300 ns total.</p>	Sten Hansen	
EED-00081	S. Pordes	3/5/2003	6/1/2003		<p>Install 9 relay racks to support new Beam Position Monitors (BPM's). Racks to be installed in six different locations around the Recycler Ring. Each rack is to house at minimum, two 6U Eurocard (VME) subracks containing new electronics, associated power supplies for the subracks, transition panels for cable connections, bias voltage power supplies for the BPM's and necessary protection, safety and monitoring equipment. A large number of cable extensions (supplied by the Computing Division) must be dressed, labeled and organized to insure high reliability and ease of maintenance. Close coordination with Beams Division and Computing Division personnel is required as the proposed schedule indicates that parts from which the racks are to be assembled shall be available no more than one month prior to the delivery date.</p>	John Foglesong	
EED-00082	William Wester	5/27/2003	10/31/2003	50	<p>Parts to be ordered under Project Task 50.01.01.03.01.</p> <p>Personnel required include those involved with Jim Hoff's SEU tolerant register radiation study including Rod Klein and people to help enter schematics and produce a printed circuit board.</p> <p>See Attached Sheet.</p>	Jim Hoff	
EED-00083	Ray Stefanski	6/4/2003	8/30/2003		<p>A rough estimate of the cost for a prototype system comprised of 12 sensor cards and 1 driver card is \$500 in parts, \$1000 for PC board fab and 2 months of engineering co-op labor and 2 weeks of Terry Kiper's time to do software.</p>	Sten Hansen	
EED-00084	William Foster	5/13/2003		20.14.1.1	<p>Review design of PCB and produce PCB for board designed by Foster and company that will be used as damper controller.</p>	Sten Hansen	6/6/2003

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EED-00085	William Foster	2/13/2003		20.14.1.1.10	Assemble and test of PCB designed by Foster and company that will be used as damper controller.	Sten Hansen	3/11/2004
EED-00086	Claudio Rivetta	5/28/2003			Design the digital readout section for a Precision Phase monitor of the TeV beam.	Claudio Rivetta	
EED-00087	Hogan Nguyen	6/11/2003			Assist with the testing of 4 channel QIE DAC board test proof of concept of Beam Ionization profile plate monitor.	Kwame Bowie	
EED-00088	Pierrick Hanlet	6/1/2003			E907 is reusing the E690 preamp/discriminator electronics. The test stand at Lab 6 is too noisy and cannot test the discriminator cards. Assistance requested to determine cause of noise and effect solution. Estimated time: 1 month	John Anderson	
EED-00089	Bob Webber	3/25/2003			Design and produce interface cables between Recycler Ring beam position monitor cabling and new BPM electronics. Label and install cables in buildings MI10, MI20, MI30, MI40, MI50 and MI60. Scheduled installation period: June 2003. Estimated time: 4 months	John Foglesong	
EED-00090	Gary Drake	1/1/2003			Procure and test low voltage power supplies for MINOS CALDET run. Design cabling harness to connect supplies to VME racks. Deliver to CERN and supervise installation on site. Estimated time: Until Q4 or 2003	Dave Huffman	
EED-00091	Marcel Demarteau	6/1/2003			Receive, test and install ~200 channels of high voltage destined for use in RUN IIB silicon detector. Label and inventory separately as these were not purchased with Fermilab funds. Estimated time: 1-2 months	Benjamin Abraha	
EED-00092	Marcel Demarteau	1/1/2003			Specify, procure, test and install low voltage power supplies for the run IIB silicon detector. Perform primary installation at 1%/10% test stations with actual system wiring to determine performance prior to final installation in detector. Integrate CAN bus monitoring of supplies into D0 monitoring system. Estimated time: 1 year	Linda Bagby	
EED-00093	Sergei Lusin	1/1/2003			Analyze CMS technical design report for DC power supply needs and provide next level of detail in system design. Determine likely commercial vendors. As requested, procure/develop and test potential solutions. Possible expansion into design project. Estimated time: One year?	Dave Huffman	
EED-00094	Ed Barsotti	6/11/2003			Provide review and input to BTeV technical design report sections covering experiment infrastructure. Identify potential work for Infrastructure group should experiment be approved for construction.	John Anderson	

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EED-00095	Ed Barsotti	6/27/2003	9/5/2003		<p>A second Director's (Temple) Review of BTeV is planned for this coming September. BTeV has eleven Level 2 Subprojects, WBS 1.1 through WBS 1.11, System Installation, Integration and Commissioning, contains sections dealing with the procurement, installation, integration and commissioning of electrical and electronics infrastructure components at C0. These components include but are not limited to such items as clean and normal AC power and its distribution, detector grounding, electronics racks and rack protection, personnel and equipment safety related to electrical and electronics infrastructure components. The Electrical and Electronics Infrastructure requirements and plans at C0 need to be documented as part of BTeV's TDR. Corresponding cost and schedule electrical and electronics infrastructure WBS Activities in WBS 1.10 need to be reviewed and updated where needed.</p> <p>This work request is a) to assist BTeV personnel in writing the TDR section of the electrical and electronics infrastructure at C0 and b) to assist BTeV personnel in reviewing and updating the electrical and electronics infrastructure section of BTeV's WBS structure, specifically related sections of WBS 1.10 described above.</p> <p>It is requested that John Anderso and other personnel who work with him be used for this work.</p> <p>It is believed this work should take no more than four to six FTE-weeks of effort between the request date (see 'Date of Request') and early September (see 'Date Required By').</p> <p>Contact People: Ed Barsotti, Chuck Brown and Joel Howell are BTeV contacts for the above work.</p>	John Anderson	
EED-00096	S. Pordes	8/13/2003	8/14/2003		<p>Request Curt Danner (specifically) to help Ron Miksa complete the electronics for an Optical Transition Radiation detector assembly. This project is behind the desired schedule and we very much would like the OTR to be tested with beam before the shutdown. I believe this is about 5 days of work and apologize for the crisis nature of the request.</p> <p>Vic Scarpine (2571, ldp 218-4095) is the physicist actually doing the OTR.</p>	Curtis Danner	
EED-00097	S. Pordes	1/20/2004	9/20/2004		<p>Support specification, design, construction, testing, documentation and installation of controller and signal processing chassis for new beam loss monitor system. The Tevatron system contains approximately 250 loss monitors distributed in 24 houses around the ring. An appropriate time for installation of complete system would be summer shutdown with successful demonstration of a significant subsystem (~10%) beforehand. A proper requested schedule should be developed jointly.</p>	Alan Baumbaugh	
EED-00098	Howard Budd	2/10/2004	4/20/2004	85.04.33.12	<p>We would like to have the department build 10 readout boards for the existing trip chip. The purpose of the board is to determine if the existing TriP chip will work for the proposed MINERvA experiment. We will be testing out the boards for both ADC and TDC information. A board will readout 16 channels of the MINOS Near Detector PMT box. The board will have a female DB37 connector and be approximately 2 3/4 inches by 4 inches. The budget code can be used to purchase the boards and parts.</p>	Paul Rubinov	

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EED-00099	Ed Barsotti	3/1/2004	3/17/2004		<p>Here is a list of work we need help on --- rather quickly if possible. In about 2 to 2-1/2 weeks most all of the documentation for the Directorate's pre-CD1 review of BTeV has to be done:</p> <p>1) High-voltage power supplies: a) Take information from CAEN quote and generate a table with requirements, costs, modules, subracks for each HV supply for each of the six detector subsystems b) Review and edit, where needed, WBS Dictionaries and Basis of Estimates c) Generate costbook (backup) material (including simple layout block diagram)</p> <p>2) High-voltage cabling: a) Generate table as in 1a with type, cost, lengths (In about FY2002 Stan Orr had done some of this work) b) Same as 1b c) Same as 1c</p> <p>3) Low-voltage power supplies: a) Same as 1a with the exception that quotes are needed. b) Same as 1b c) Same as 1c with the addition that credible backup material regarding radiation and its effects on the supplies is needed. Perhaps some words about shielding the supplies with steel is sufficient.</p> <p>We have a very good start with HV but LV needs a lot of work. We're thinking of putting the HV supplies just outside the collision hall just above the large entry door. The LV supplies would be in the collision hall.</p> <p>Will Johns from Vanderbilt is to have low-voltage current, voltage and regulation requirements for the six detector subsystems by this coming Wednesday.</p> <p>What we're looking for are credible implementations and credible costs with sufficient backup material.</p> <p>I would estimate that 2-1/2 weeks of elapsed time and 1 to 1-1/2 weeks of effort is needed --- but we need that person, if you have him/her to help us NOW and he/she needs to be done within 2 to 2-1/2 weeks.</p>	Pat Liston	

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EED-00100	Dan Bauer	1/30/2004	4/1/2004		<p>Design, assemble, test and install a Power Supply Interface Chassis for CDMS</p> <p>Here are a few details to add. The interface box would live in one of the electronics room racks, probably near the FEB power supplies. The PCI digital I/O card for power supply control and status is a PCI-DIO24H. I've attached the manual to show the connector (D37) and specifications (made to drive and read TTL levels). There would be one cable between this card in one of the DAQ PCs and the interface box; it would have to be 30-40' long.</p> <p>In addition, there would be cables between the interface box and each of the 8 power supplies you mention. Finally, we should allow for 2 cables from the RF room for the fan interlock lines (just in case we have separate interlock boxes for the two FEB relay racks that we ultimately will have).</p> <p>Dan</p> <p>on 1/30/04 10:43 AM, Wayne Johnson at wjohnson@fnal.gov wrote:</p> <p>Dan and Stan,</p> <p>As i recall from our conversation here are the quick notes that I have for the Power Supply interface.</p> <p>Build an Interface Box for the CDMS Power Supplies.</p> <p>The Box will have the following capabilities to support up to 4 FE Power Supplies and 4 RTF Power Supplies.</p> <ol style="list-style-type: none"> 1. Power Supply Remote Start/Stop. Application of momentary +5 V. 2. Remote Status monitoring. 3. Interlocking to Cooling Fan monitoring system, both fan operation and power supply status. <p>Please add or delete as you know to these basic notes.</p> <p>Thanks,</p> <p>Wayne</p>	Wayne Johnson	
EED-00101	Mike Crisler	7/8/2003			<p>Downgrade of CDMS STM</p> <ul style="list-style-type: none"> - Simplify Controls - delete 4 port memory - use internal bus 16 data, 8 address, 8 control - architecture as noted on attached sketch 	Mark Kozlovsky	
EED-00102	Simon Kwan	7/2/2003	9/2/2003	40/40.22.04	<p>Layout of a prototype vacuum feed through board for the BTeV pixel detector.</p> <p>We will need the first 1/4 station section completed by early September so that we can get a quote and have the P.O. in place before the end of the Fiscal Year.</p> <p>For details: See BTeV-Doc 1730</p> <p>Technical contact: Brad Hall X6599; bhall@fnal.gov</p>	Mark Kozlovsky	
EED-00103	Andreas Jansson	3/25/2004		20/20.1.1.16	<p>Tevatron IPM Front End Card</p> <p>Design and build a front end card for the Tevatron IPM using a QIE chip.</p> <p>See Attached Specs.</p>	Kwame Bowie	
EED-00104	Andreas Jansson	3/25/2004		20/20.1.1.16	<p>Tevatron IPM Clock distribution card.</p> <p>Design and build a clock and timing module for the Tevatron IPM.</p> <p>See Attached Spec.</p>	Tom Fitzpatrick	

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EED-00105	Rajendran Raja	4/14/2004			We need to turn off 6 Glassman HV power supplies used to supply HV to the MIPP/RICH if one of the tubes spark. The spark is of duration ~25-50 microseconds. The peak current in the spark is of the order of a few amps. The supply has an interlock which can be dropped by the spark detection circuit. The supply that is switched off thus should be flagged by turning on a red LED. The interlock is reset by power cycling the supply.	Sten Hansen	
EED-00106	Bruno Gobbi	4/21/2004	9/1/2004	400 5.11.1.3.3	<p>Update ASIC tester box for high speed data transfer in wafer testing of CMS pixel devices. The understanding is that boards already exist and that some components will need to be order to complete assembly of the boards. It is also understood that personnel resources will be required to program and debug the boards so that they can be used for pixel testing.</p> <p>We will do the following (Wm. Wester)</p> <ul style="list-style-type: none"> -Finish building and then debug a new board for the tester box with a faster link to the DAQ computer. - Write software to support this higher speed data transfer. <p>Specifically, there would be time charges for Al Baumbaugh (Eng) and Kelly Knickerbocker (Tech) and some parts charges. The new board already has been designed and produced and is in hand. The improvements would be done to be compatible with the rest of the existing software. The main improvement will be that you will have more complete testing information on the pixel level with this system.</p>	Alan Baumbaugh	
EED-00107	Mike Crisler	4/22/2004			Provide two electrical technicians for temporary reassignment to Accelerator Division Electron Cooling Project. Technicians will participate in the disassembly of the Pelletron and its associated beamlines in Wide Band and in the packing, transport, and re-installation at MI-31. Work will be under the supervision of Kermit Carlson. Work is underway and is anticipated to continue through calendar 2004 (roughly 7 months is the estimate).	Wayne Johnson	
EED-00108	Alan Stone	4/29/2004	7/1/2004		<ol style="list-style-type: none"> 1. Measure and determine appropriate termination required to connect existing Calorimeter pickoff signal cables (ribbon coax) to new L1 Cal Trig boards. New boards plan to use a double shielded twisted pair cable configuration. 2. After determining correct connection/termination scheme, develop patch panel to connect old cables to new cables with appropriate termination. <ol style="list-style-type: none"> 2.1. Patch panel is also to provide easily accessible test points for end user scope probe connection. 3. Manufacture and install 5 patch panels into D0 movable counting house. Installation to include connection of all cables. <p>Supplementary documentation available at</p> <p>http://www.pa.msu.edu/hep/d0/ftp/run2b/l1cal/hardware/adf_2/general/bls_to_adf_backplane_extension_cables.txt</p> <p>http://dzero.phy.uic.edu/mario/trigger/Run_IIB_L1CAL_Cabling.pdf</p>	Johnny Green	
EED-00109	Tom Jordan	5/7/2004	9/4/2004		<p>We propose to make between 100-200 additional QuarkNet readout boards identical to the version designed by Sten Hansen and under production in Bob Jones' shop just now.</p> <p>We request the same testing agreement that is currently in place, i.e., Curt Danner checks the board using the same algorithms he is currently using before delivery.</p> <p>We plan to have the boards etched offsite. Depending on overhead costs, we may acquire board components and deliver them to Bob as we have done in the past, or we may ask Bob to order the parts.</p>	Curtis Danner	

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EED-00110	Alan Stone	5/15/2004	8/15/2004		<ul style="list-style-type: none"> · Determine best method to connect existing ribbon coax cables (75 – 80 ohm Zo) to new ADF trigger cards with incompatible connector layout. <ul style="list-style-type: none"> o Insure new connection minimizes errors due to reflection from impedance mismatch o Provide accessible scope probe test points on each cable · Specific work requested after discussions: <ul style="list-style-type: none"> o Design/build 'patch panel' PCB to connect extant cables to ex-tender cables o Build/obtain sufficient quantity of pleated foil ribbon cables to act as extenders o Design/build 'paddle card' PCBs to connect pleated foil cables to rear connector of new ADF cards <p>Supplementary documentation available at:</p> <p>http://www.pa.msu.edu/hep/d0/ftp/run2b/l1cal/hardware/adf_2/general/bls_to_adf_backplane_extension_cables.txt</p> <p>http://dzero.phy.uic.edu/mario/trigger/Run IIB L1CAL Cabling.pdf</p>	John Foglesong	
EED-00111	S. Pordes	5/28/2004	7/23/2004		<p>Provide programming for FPGA in BLM Digitizer board (see Beams Document Data Base - http://beamdocs.fnal.gov/cgi-bin/public/DocDB/ShowDocument?docid=1131&version=1)</p> <p>The FPGA is used to accumulate sums of values from ADC's and compare sums to threshold values and to control a DAC. Craig Drennan is the engineer on the board and will provide complete specs. We would like to test a version of the board on beam before the shutdown which is scheduled to start August 23rd 2004 - hence the date required by.</p>	Cecil Needles	
EED-00112	Gary Drake	4/1/2004			<p>This request is to design an integrated circuit called DCAL that can be used to readout 400,000 channels of RPCs and some GEMS if possible. The general design concept was outlined by Gary Drake in an initial document titled "Lin-ear Collider Digital HCAL, Electronics for Resistive plate Chambers" dated 2/27/04. The engineering design work will be funded by Fermilab as a Linear Collider effort. The chip fabrication will be fully funded from Linear Collider money from Argonne. Each prototype could cost about \$20K. Two prototype runs are expected. A full size prototype is expected in 2005. A production quality device may not be ready until early 2006.</p>	Jim Hoff	
EED-00113	Alan Hahn	5/1/2004	1/1/2005		<p>Design TDC ASIC for BTEV straw detector. Preliminary specifications are specified in TDC/SI ASIC block diagram, CD1 Review dated April 27, 2004. Chip will be designed in TSMC 0.25u process, but since radiation is limited to 100 krads over 10 years, enclosed geometries will not be used in order to simplify the design.</p>	Ahmed Boubeke	

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EED-00114	Alan Bross	6/29/2004			<p>Redesign existing Trip chip ASIC to include hit timing information for the scintillating tile calorimeter at Dzero. The new chip called Trip-T will be used on the new AFE II boards. Paul Rubinov wrote a set of preliminary specifications for the Trip-T dated Jan 20, 2004. These are meant to be a guideline and could change during the design phase. The redesign is expected to begin about June 1, 2004. The question of proper pipeline operation needs to be immediately resolved. Assuming the pipeline problem can be resolved quickly, a prototype design is targeted for submission on August 23, which is the closing date for a TSMC 0.25u run at MOSIS. The submission should be a complete chip design.</p> <p>TriP-T chip specifications (preliminary) -----</p> <p>Revised: 20 Jan 2004 by PMR based on original specs for TriP by PMR and Bruce H</p> <p>Note: All charges throughout this document, are at the VLPC. The interconnect from the VLPC's and the TriP chip is described below.</p> <p>Note: We are flexible. If designer suggests changes we will look into it.</p> <p>These specs are very similar to those of the TriP with the following changes:</p> <p>Bunch crossing rate = 396 ns. This gives the chip much more time in reset.</p> <p>We wish to add a Time to Voltage converter: This function should allow us to measure the time of the discr firing relative to some clock over a range of no less than 120ns with a resolution of about .58ns In other words, if the time range from 0 to 120ns corresponds to an output of 0 to 1.2V, then the RMS voltage noise should be less than 5.8mV. This is required if the effective LSB is to be at 2ns after digitization.</p> <p>The outputs of the T-to-V converter should be delayed by the same pipeline as the output of the integrator and should be muxed out the same pins and the same way as the integrator analog outputs.</p> <p>Other tweaks: We expect the VLPCs and the fibers to degrade over time, so I lowered typical signal at high gain to 32fC and 6 pe. I also lower the max signal before saturation to 150fC from 300fC because we are currently working in a mode where the signal saturate at about 75 or 80fC with little complaint. I also reduced the max test input charge- this cap is a parasitic on the input and should be kept small.</p> <p>Channels = 32 trigger + 32 analog</p> <p>Window for charge collection: from 50 to 150 ns controlable by width of clock pulse. The typical integration width we expect to use is 100ns. All noise measurements will be made with this integration window.</p> <p>Temperature range = 10 degC to 50 degC.</p> <p>One adjustable gain setting per chip. All channels same gain (from G/2 to G*4 in steps of G/2) 4 bit control (feedback capacitors C, C, 2C, 4C, 8C).</p> <p>Input signal from Fiber Tracker or MIP layer of Preshower Detector (at high gain): min: 1 photoelectron at 90 degrees incidence = 4 to 9 fC</p>	Abder Mekkaoui	

typ: 1 MIP = 6 photoelectrons = 32 fC for Fiber Tracker
 1 MIP = 65 fC for MIP layer of Preshower Detector
 max before saturation = 150 fC

Threshold setting for Fiber Tracker and MIP layer
 of Preshower Detector (at high gain):
 from 0 to 100 fC with 7 bit control (linear)
 typ: 4 to 20 fC
 99% of channels within +-4 fC
 rms noise < 1.0 fC
 temperature coefficient < 2 fC/10 degC

Input signal from shower layer of Preshower Detector
 (at low gain = high gain/16):
 typ: One 40 GeV electron or gamma at 45 degrees = 25 MIP per strip
 = 450 photoelectrons = 1890 fC

Threshold setting for shower layer of Preshower Detector
 (at low gain = high gain/16):
 from 0 to >500fC with 7 bit control (linear)- this is a best effort number. T
 The max threshold setting should be as large as possible without compromising
 other chip parameters
 typ desired: 100 to 750 fC.

Power consumption < 10 mW per channel.

Inputs:
 same as for TriP

Analog outputs:
 32 channels with 2 16:1 analog multiplexers, balanced
 readout occurs in readout mode (not during acquisition mode)
 readout rate = 7.6 MHz
 channel uniformity should be within +-3%,
 i.e. +-0.03x300 fC = +-9 fC referred to the input at high gain
 ch rms noise < 1 fC referred to the input
 temperature coefficient < 2% of full scale/10 degC
 external load approx 10 pF

Digital outputs:
 32 channels with 2:1 digital multiplexing for 16 unbalanced outputs,
 with adjustable current limit (or rise time controlled)
 output in acquisition mode and only during integrator reset
 standard: LVCMOS2, 2.5V
 external load approx 10 pF.

Test input:
 negative charge from 0 to 200 fC (for gain G)
 pulse time and width determined by CAL-INJECT
 pattern settable

Pipeline depth:
 47 buckets programable from 0 to 47.
 (existing SVX4 pipeline)

Power supply: +2.5V, digital separate from analog.
 Power supplies should require no sequencing (if possible)

The chip will be packaged.

Clocks provided to chip:

- 1) 132 ns period with settable duty cycle,
LVTTL high (approx. 2.5V) for charge acquisition window,
LVTTL low (approx. 0V) for reset.
 - 2) LVTTL high during discriminator bucket A readout.
 - 3) LVTTL high during discriminator bucket B readout.
- All other clocks needed in the chip for acquisition
and readout to be derived from these.

Analog output will be digitized by AD9201.

The input voltage span of the ADC is 0 to 1V.
The output of the chip will be referenced to ground
or it should be differential.

Decoupling capacitors: The inputs to the chip are
negative going. Therefore the VLPC charge loop
includes AVDD and AGND. Therefore several AGND-AVDD pad pairs
will be needed to place decoupling capacitors.

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EED-00115	Ed Barsotti	8/12/2004	10/1/2004		<p>Ed requests that Pat Liston and I work to develop two sets of documentation for BTeV's upcoming CD2b/3a Lehman review regarding low voltage power supplies. His base desire is that Pat develop a cost structure for all BTeV low voltage requirements based upon a 48V main distribution and subsequent DC/DC converters, and that I develop a cost structure for comparison using 110/220VAC commercial switching supplies. The intent is to end up with one detailed cost structure and implementation scheme sufficient for use in the upcoming CD2b/3a review.</p> <p>Ed's original email request is a classic, so here it is as reference material (note the time sent and the requested delivery date!). He references a document in the BTeV document database. This is achieved by going to http://www-btev.fnal.gov, clicking on BTeV Internal (Ed gives the username and pass-word below), then entering the BTeV Document Database link and selecting his document by its document number.</p> <p>Date sent: <input type="checkbox"/> Thu, 12 Aug 2004 06:18:18 -0500 From: <input type="checkbox"/> Ed Barsotti Subject: <input type="checkbox"/> Distributed 48V system --- requesting your help To: <input type="checkbox"/> janderson Copies to barsotti</p> <p>John,</p> <p>I'll be away today. Last night I spoke to Joel and he gave me the green light to officially proceed with preparing a note and presentation (technical and cost) to get the distributed 48 volts with on-board and/or near-board DC-DC converters and/or regulators for BTeV's low-voltage power supply system (Boy, that was a long sentence!). I need your help. With BTeV's rapidly-approaching CD2/3a Director's review then the Lehman review, we have VERY little time to a) propose the system, b) get it approved, c) get the changes in the WBS, and d) write backup material.</p> <p>I'll be sending you e-mails of budgetary quotes, etc. of 48V sources from Power One (pay attention only to the one from Scott), budgetary quotes, etc. of DC-DC Converters from Power One (Mike Rita) and some other e-mails. Note on the latter that Mike only sent 48V to 12V and 12V to ??? volt converter information where he was supposed to send 48V to 12V and 48V to ??? volt converter information. I'm asking you to quickly get from another company part and price guesses for the latter. Assuming you can access BTeV's document database (username: and password:), please access my presentation (document #3305), read it over, etc. Note it has a table of current power needs guesses. I've added about 25% to those guesses when discussing needs with Power One.</p> <p>Can you start/do the following today in preparation for our meeting Friday?</p> <ol style="list-style-type: none"> 1) Read over all the information 2) Get type and costs for 48V to ??? volt DC-DC converters 3) Get type and costs for linear regulators (Linear Technology?) (I'm also sending you ST Microelectronics info on rad-hard regulators being built for LHC) 4) Start preparing a (Excel?) summary sheet of costs, etc. for BTeV assuming we only power 25% of counting room electronics and 100% of collision hall electronics with this system (processors are bought with their own supplies 5) Start preparing a document on the implementation 	Pat Liston	8/12/2004

6) Rest

Thanks in advance,

Ed

EED-00116	Jim Williams	8/18/2004	1/1/2005		Reverse engineer the AMETEK leak detector for the Technical Division Magnet Facility. Dan Schoo will consult on this job but we will need an engineer to oversee the project. There are 4 boards that are one-sided and not very dense. A parts list and estimate of work will need to be made first before the project will get a division approval. Ultimately, these leak detectors will be produced on the outside after a prototype is built and tested by the PPD/EED group.	Xinyi Chen
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EED-00117	William Foster	1/28/2004	1/1/2005	20.13.1.2.8	<p>I believe that everything is sufficiently well defined that work on the front end of the board should be able to start almost immediately.</p> <p>There are a few semi-self-contained subdesign design tasks that are off of the main line of development of the board, that I would like to try finding someone (besides you!) to spin off to, so as not to have them slow down the design effort.</p> <ol style="list-style-type: none"> 1) to find out how the 2GByte SDRAM module interfaces to the Stratix, and try to figure out if there is any strategy to avoid having it spray TTL noise all over the analog front end. 2) See what's feasible for GBit Ethernet implementations with the Stratix part, including compiling the "firmware CPUs" needed to support the protocol. 3) Coordinate with the LLRF guys (Brian Chase and family) to understand what the SHARC implementation has to be like to maintain software compatibility with their current setup. <p>Also if it works out OK I'd like to have Charlie Nelson look over your shoulder on the analog front end. On this implementation I've called for (of course) the newest best fastest Analog Devices DAC, and some of the potential applications (broadband LLRF outputs to storage rings) call for the quietest and most stable and precise DAC output as well as the as well as low ADC noise. So for example it might be a good idea to use separate small-footprint series regulators on each DAC & ADC channel, rather than single regulators getting really hot at the edge of the board and bazillions of surface-mount inductors to isolate the power supplies. (also, the individual regulators might not burn out each time you momentarily short out the power supplies with a probe...) anyway, Charlie is really good at this stuff and besides then when the first version of the board is way noisier than it should be you can both blame it on me.</p> <p>-Bill Foster</p>	Marcus Larwill
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EED-00118	Marvin Johnson	8/30/2004	9/13/2004		<p>The request is for engineering support to commission the DZERO Forward Proton Detector Level 1 Trigger. This task involves firmware simulation and implementation for the DZERO Digital Front End (DFE) boards designed for the Central Fiber Tracker (CFT) Trigger. Data from the FPD Scintillating fiber detectors is read-out by analog front end boards (AFE), discriminated and passed to DFE boards. Hit pattern algorithms need to be programmed into the DFE boards and interfaced with DFE control firmware. The DFE information is then sent to muon-type trigger manager boards for use in L1 triggers. More documentation is available at http://d0server1.fnal.gov/users/ramirezg/www/l1fpd/index.html</p> <p>Estimated 6 months at 50% time required to complete job.</p>	Tom Fitzpatrick
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EED-00119	Sergei Lusin	10/5/2004	6/1/2005		<ul style="list-style-type: none"> · Develop prototype 48V, 1.5kW power supply for use at CMS. Supply design is subject to the following special requirements: <ul style="list-style-type: none"> o Must be powered from 220VAC, three-phase, 400Hz. o Must operate to specs within 1000 Gauss magnetic field. o Must be radiation tolerant. o Shall interface to CMS slow controls using CAN bus interface (ideally, using internal ELMB board used elsewhere at CMS & ATLAS) o Required to fit within space (length, width, height) as defined by CMS. o Proof against short-circuited outputs o Minimal conducted noise on AC lines (defined as < 10% THD, < 5% THD preferred) · Manufacture small number of supplies for use at CMS as prototypes. · Redesign supply after prototype tests for mass production (approximate quantity, 300) at outside assembly firm. · Concurrent development of 48V, 3kW supply prototype (dual supply) with same operational restrictions as original design above. 	Dave Huffman	
EED-00120	Brenna Flaughner	12/22/2004	6/1/2009	40.38.01	<p>I am requesting support for the development of the Front End Electronics for the DES project. This includes overall system design of the interface between the CCDs and the Data acquisition system. It also includes support for the CCD testing efforts: design, fabrication and testing of adapter boards, cables + connectors, controller interfaces and associated electrical systems. It also includes the design and development of a slow control system for the camera, which will interface with the telescope control system and the DAQ system. I would like Fermilab to be in the position of leading these efforts and guiding/organizing the contributions from the various collaboration members.</p>		
EED-00121	Richard Smith	1/7/2005	2/1/2005		<p>Recent trouble with the Dzero solenoid magnet has resulted in a need for continuous monitoring of the voltage drop across the various tap points of the solenoid. A temporary solution consisting of an amplifier box and a networked chart recorder shows that a measurement system with 10uV resolution clearly shows changes in voltage consistent with models of the quenching problem.</p> <p>Development of a 16-channel differential amplifier with 10uV sensitivity in each channel, low-pass filtering with a corner frequency of 4Hz or less and sufficient output drive to interface with a commercial 16-channel, 16-bit $\pm 10V$ PLC input module is requested. Two units (one for use in the collision hall, one as a spare) are desired. All channels shall be individually tuned for minimum output offset for zero input. Characterization curves of gain, frequency response and offset for each channel are required.</p> <p>The amplifier box shall be powered by its own DC-DC converter "brick" power supply, housed in a metal chassis and be installed in the Dzero collision hall. The job shall include specification and installation of the cable plant from the amplifier box to the existing cryo control system, procurement & installation of the 16-channel PLC input module and coordination with the cryo control technicians to include continuous monitoring of these channels in the Dzero control room GUI and system logs.</p>	John Anderson	

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EED-00122	Nikos Varelas	1/31/2005			<p>Provide infrastructure assistance to L1 Cal upgrade project, specifically the following:</p> <ol style="list-style-type: none"> 1.□Setup of "sidewalk" test stand including assembly of relay racks, installation of user equipment into relay racks, AC power distribution and monitoring to allow safe unattended operation. 2.□Develop methodology to test all cabling patterns necessary in final installation on "sidewalk" test stand. 3.□Work with L1 Cal physicists to integrate monitoring and control of new L1 Cal electronics into existing Dzero system. 4.□Develop plan for deconstruction of existing L1 Cal system in 1st floor movable counting house and installation of new L1 Cal system into the same relay racks. 5.□Provide and supervise technician labor necessary to accomplish items 1-4 above. 6.□Provide, as necessary, engineering support (expertise, test equipment, etc.) to assist post-docs testing new L1 Cal equipment on the "sidewalk" test stand. 7.□Continue to develop web-based documentation generated as part of task EED-00110 to cover all items above. 	Linda Bagby	
EED-00123	Jonathan Lewis	3/2/2005	6/30/2005		<p>Design and fabricate Control Card for Accelerator BLM upgrade. To ensure that data communications and other tasks running on the VME crate computer do not impact the reliability of the BLM abort logic, the Control Card (CC) provides an independent dedicated eZ80 processor that manages the setting of abort thresholds and other parameters used in the abort logic. The CC communicates with the other system cards over the dedicated custom J2 backplane keeping local communications separate from VME data transfers. The CC also maintains circular buffers that store the histories of the three running sums for each digitizer channel. The history can be read out via VME by the front-end processor. The CC also stores abort thresholds for each of the sums for each channel for up to 256 machine states. Further information can be found in http://beamdocs.fnal.gov/cgi-bin/public/DocDB/ShowDocument?docid=1410&version=4.</p> <p>We require three prototype modules for integration testing by 15 April 2005, and a production quantity of 43 by 31 August 2005.</p> <p>[Note: The schedule as requested (6.5 weeks to functioning prototypes) is more aggressive than EED will be able to achieve. We will proceed as quickly as we can. - RJD]</p>	Jin-Yuan Wu	
EED-00124	Roger Rusack	10/1/2004			Design multi-channel ASIC to readout APD's. Specifications to be determined.	Tom Zimmerman	